IQVFO Performance Analysis

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Conclusions

1) The output of the AD9854 DDS is very clean. A Phase Lock Loop on the output is not necessary for HF radio applications.
2) MMIC amplifiers generate harmonics when driven at normal levels. These harmonics are still present but at much reduced levels when the MMICs are driven at a level that is much lower than rated levels.
3) When the HFVFO is used in a transmitter, band pass (or low pass) filters designed for the operating frequency range are needed to suppress harmonics.

Discussion

1) Analysis of AD9854 output signal

The spectral purity of a DDS-based VFO has been the subject of great debate in the technical community. Note that much of the discussion is related to earlier generations of DDS parts, which feature Digital to Analog converters (DACs) that are not as good as the AD9854's DAC. Nevertheless, the topic deserves serious study.

Much of the speculation in the literature and the Internet that has been centered on the spurs that are generated as byproducts of the DDS devices. Most often the speculation proceeds to the assumption that a phase-locked loop (PLL) is necessary on the output to reduce the spurs.

The AD9854 has a 12-bit DAC while previous generation DDS's had fewer bits. For example, the AD9850 has a 10-bit DAC. Additional bits in the DAC are important in reducing the undesirable byproducts (spurs). Dynamic performance (Spurious Free Dynamic Range - SFDR) improves by 6 dB with each additional bit. (See Analog Devices Application Note AN-282.) The AD9854, with its 12-bit DAC, has an 80 dB SFDR.

This performance analysis was done for the purpose of determining the spectral purity of the DDS-based VFO as implemented in this HFVFO project.

Note that the HFVFO board includes 7-pole elliptical low pass filters between the AD9854 dual outputs and the MMICs, to suppress VHF emissions. The affect of these low pass filters is ignored in this analysis. The low pass filters' cutoff frequency is 30 MHz so it only affects (attenuates) signals that are higher than 30 MHz. Since we were

trying to analyze the noise within the frequency spectrum that is lower than the LPF cutoff frequency we ignored those effects.

The output signal level of the AD9854 can be adjusted by changing the value of the resistor known as Rset. This resistor value is selected on the basis of the output signal level desired. The formula for selecting Rset:

Rset = 39.9 / Iout

The nominal value for Rset in the HFVFO is 3.9K, corresponding to an output current of 10 ma. This is in the center of the normal range of 8k (5 ma) to 2k (20 ma). Since the output load resistance is 50 ohms, 10 ma through 50 ohms corresponds to an output voltage of 500 mv RMS. Note that these output levels are not attainable when the load is not exactly 50 ohms. In this project, the load is not exactly 50 ohms when the low pass filter and MMIC are attached, so 500 mv is not observable at the junction of the AD9854 and the low pass filter.

Note that design decisions were made from the beginning of the project to maximize the AD9854 output spectrum purity. To this end, these design decisions were made:

a. The AD9854's clock multiplier was not used.
b. The frequency of the DDS reference clock (125 MHz) was selected with the intent of keeping it well above the minimum (Nyquist) frequency. The Nyquist frequency is two times the desired fundamental frequency.
c. The output drive level was kept low.
d. All unused portions of the AD9854 were turned off and the inputs were grounded.
e. Optional components that contribute to the SDFR, such as the DAC bypass capacitor and other bypass capacitors, were used.
f. Careful isolation (single connection point) was done between the analog and digital grounds of the AD9854.

With these design decisions in place, what does the output of the AD9854 DDS look like? To answer this question, an Advantest R3361A spectrum analyzer was used to produce spectral plots to demonstrate how the DDS outputs change under varying conditions.

The first plot (Figure 1) shows the signal at Header 10, after the low pass filter, and no MMIC amp in the circuit. The only harmonic that is visible is the second harmonic and it is more than 65 dB lower than the fundamental. The other harmonics are down in the low noise level. In this case, the Rset value is 3.9k ohms. The signal level is 115 mv peak-to-peak, or 40 mv RMS.

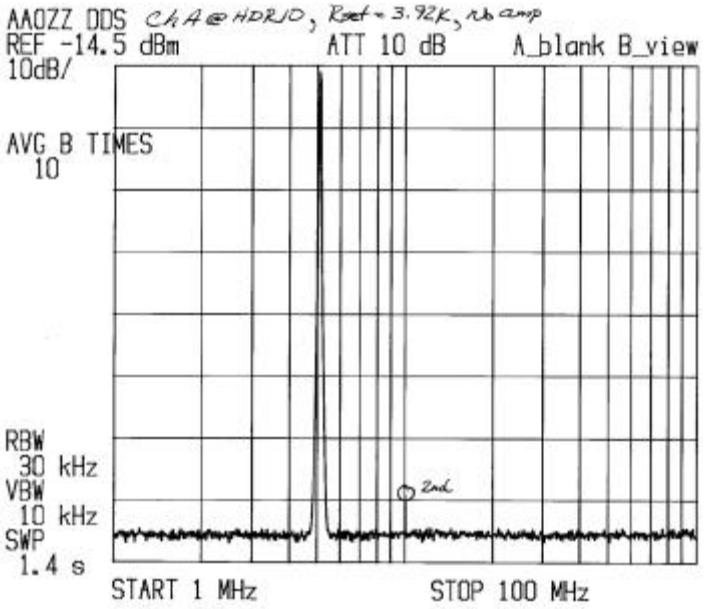

Figure 1

The next plot, (Figure 2) shows what happens when the Rset value is changed to 15k, to reduce the AD9854 drive level. It is also taken at Header 10, after the low pass filter, with the MMIC removed. With these conditions, no noticeable harmonics or spurs can be seen; the output is very clean.

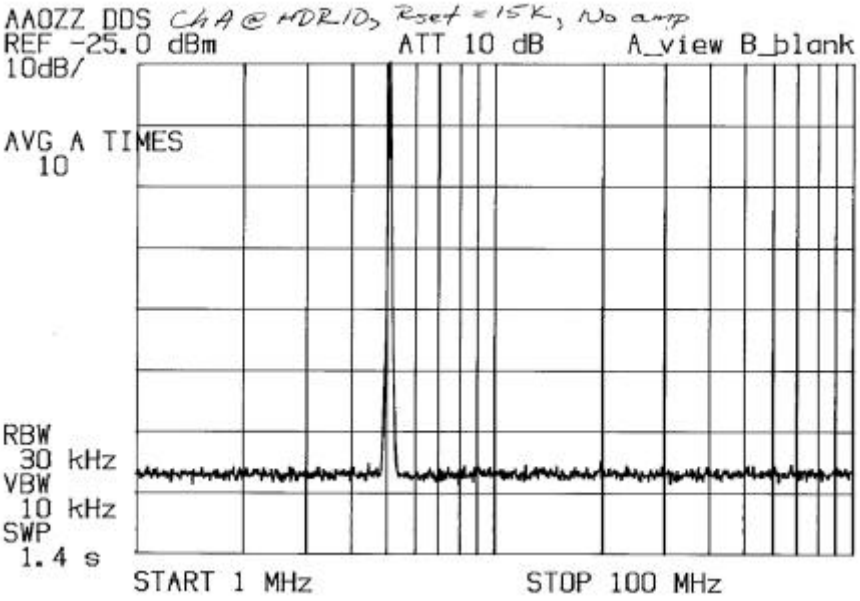

Figure 2

How about DDS harmonics/spurs? The SA output plots show they are all down 65 dB or better. This leads us to the conclusion that this HFVFO can be used as a sine wave frequency-generating source for an HF radio (transmitter and/or receiver in 1.8 to 30 MHz range) without additional filtering or PLLs to clean up the output signal. If is also evident that Rset has an effect on the generation of harmonics. Lowering the DDS output level will lower harmonics and spurious signals.

2) What does the MMIC amplifier do to the output spectrum?

The next SA plot shows what happens when a MMIC amplifier is used with the AD9854.

Figure 3 shows the output at Header 9, which is also the input to the MMIC amplifier. This is logically the same connection point as Header 10 but it is looking at the other output (channel) of the AD9854. Once again, it is after the low pass filter but this time a MMIC amplifier is connected. The second harmonic is now only 42 dB down, a degradation of about 25 dB, due to driving the input of the MMIC amplifier. Additional low level spurious outputs also appear. In this case, Rset is at 15k to reduce the drive and minimize these problems.

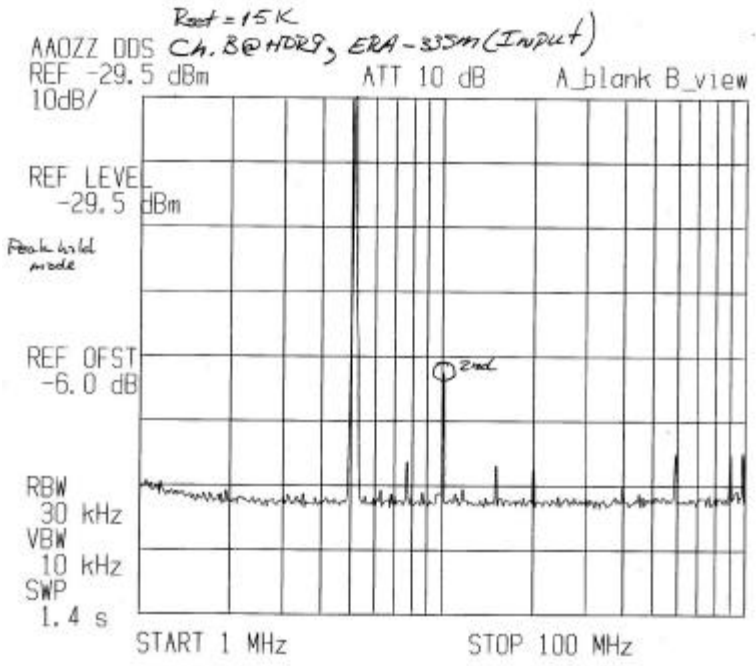

Figure 3

Figure 4 shows the signal at Header 11, the output of the MMIC amplifier. The second harmonic is now only 35 dB below the fundamental, and other byproducts are also seen. Rset is 15k in this case also. The signal level is now 2.4v p-p or 850 mv RMS (11.6 dBm).

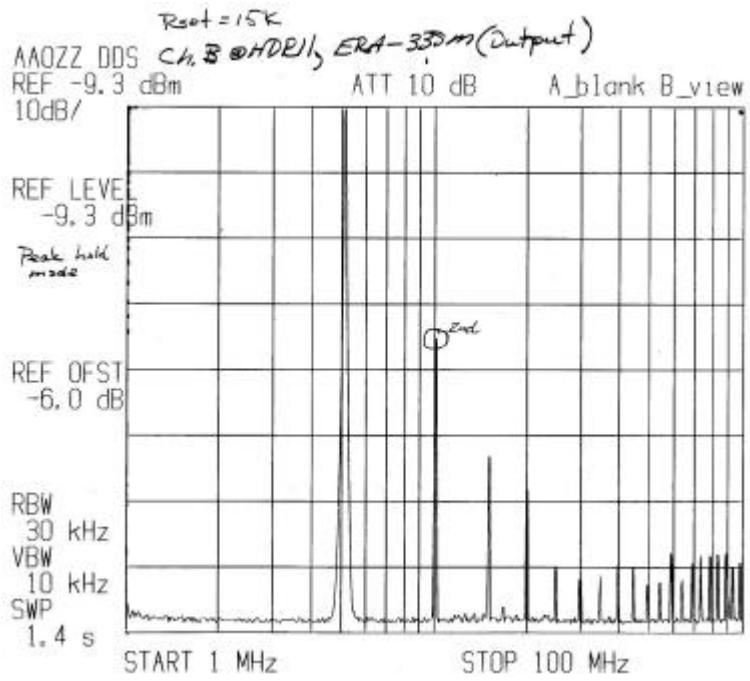

Figure 4

This leads us to the conclusion that MMIC amplifiers cannot be driven hard. If they are, the harmonic levels will be greatly increased.

Note that the MMIC used in these tests is an ESA-33SM. In other tests, the ERA-3 was shown to have similar characteristics.

3) Confirmation by Modeling the MMIC with ElectronicWorkBench

To investigate this phenomenon further, a MMIC was modeled with Electronics Workbench (EWB). Figure 5 shows the circuit that was used to represent the MMIC.

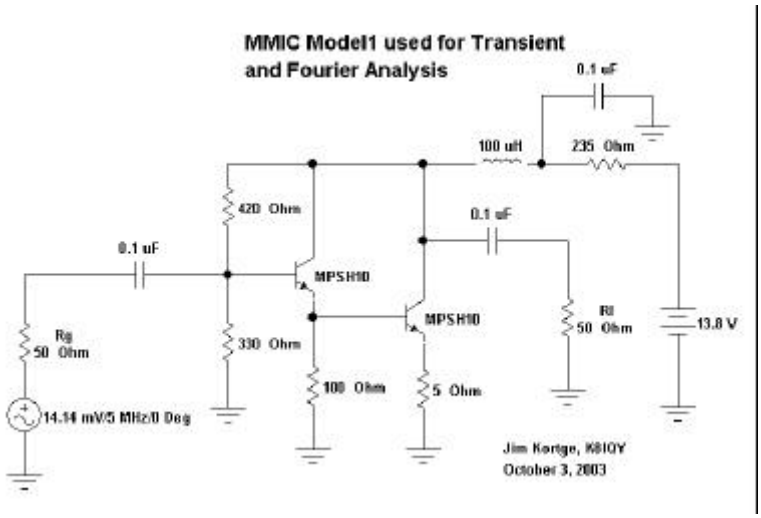

Figure 5

The generator in the simulation model is set to twice the desired input voltage since one-half of the power is consumed in the generator's internal impedance, Rg. The input of the MMIC model starts at the base of the first transistor and its bias resistors.

First, we analyze the MMIC when a input signal level of 7.07 mv RMS (20 mv p-p) is applied. Figure 6 shows the transient response of the model with this input level. The 20 mv p-p input level results in an output of 120 mv p-p.

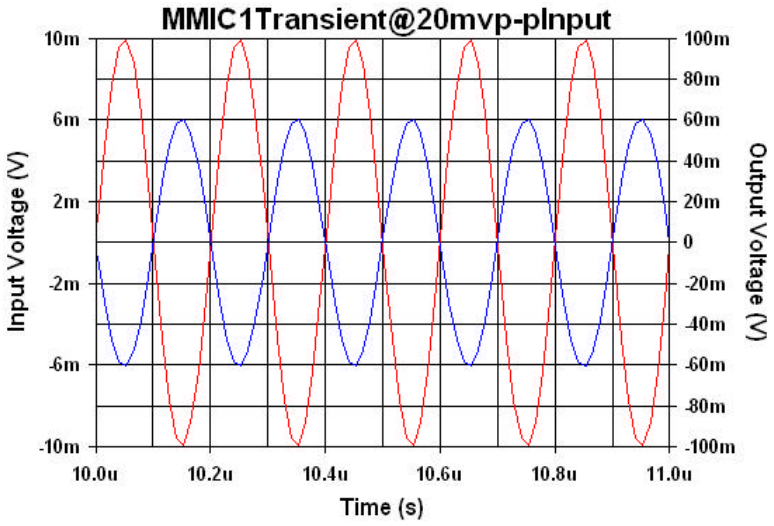

Figure 6

The modeling software can also provide spectrum analysis, showing the harmonics when this signal level is applied. The results, Figure 7, show a fundamental that has a magnitude of –25 dB, a second harmonic that is –82 dB (57 dB below the fundamental).

The third and fourth harmonics are both about –102 dB, which is 77 dB below the fundamental.

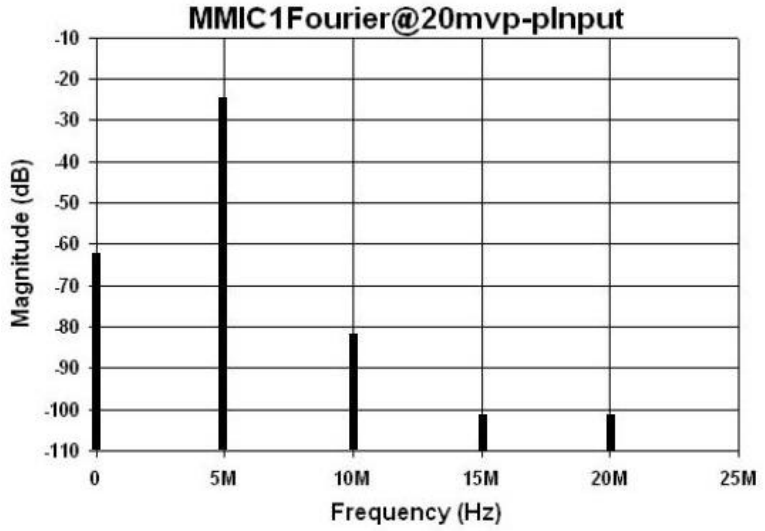

Figure 7

What happens when the MMIC is driven harder? This is answered in Figures 8 and 9. When the input is 200 mv p-p, the output is 1200 mv p-p. The spectrum analysis shows the fundamental magnitude to be –5 dBm and the second harmonic at –42 dBm, just 37 dBm below the fundamental. The third harmonic is at –61 dBm (56 dBm down from the fundamental) and the fourth harmonic is –88 dBm (83 dBm below the fundamental).

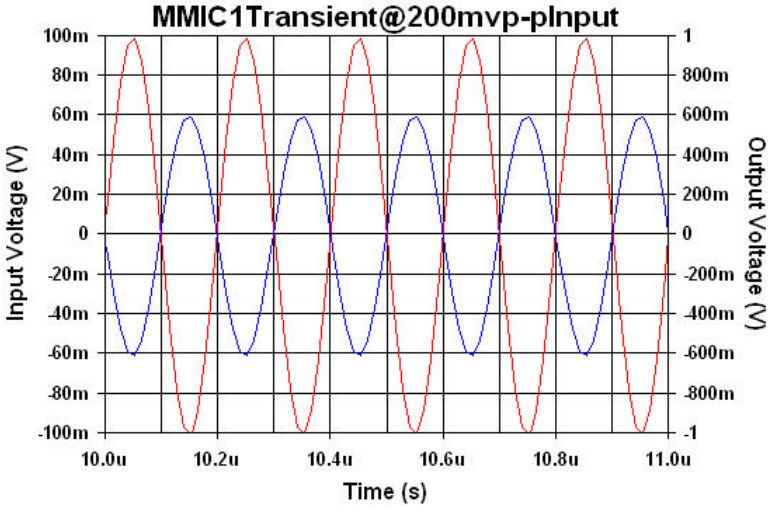

Figure 8

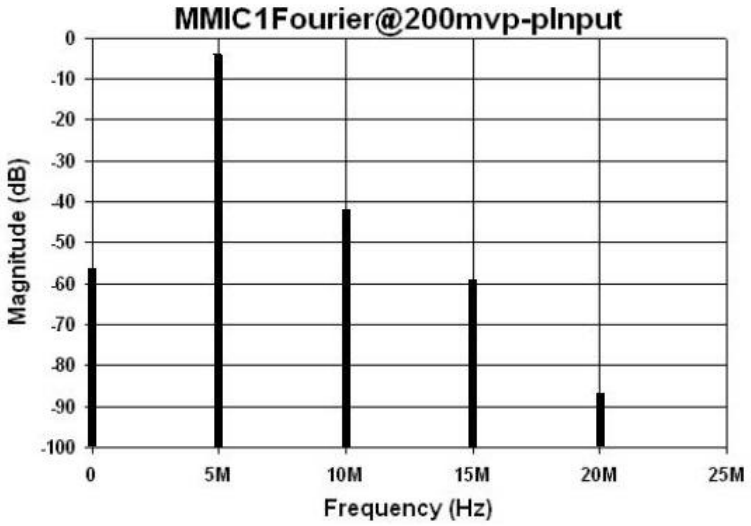

Figure 9

The harmonic levels are summarized in a chart (Figure 10) and a graph (Figure 11). The chart and graph also include values for the harmonics produced when the input drive level is doubled to 400 mv p-p. Now the second harmonic is only 28 dB below the fundamental and the third harmonic is only 38 dB down.

MMIC Model1 Performance Analysis

Input Voltage (P-P)	Output (dB)	2nd Harmonic (dB)	3rd Harmonic (dB)
0.02	-25	-82	-102
0.2	-5	-42	-61
0.4	1	-28	-38

Figure 10

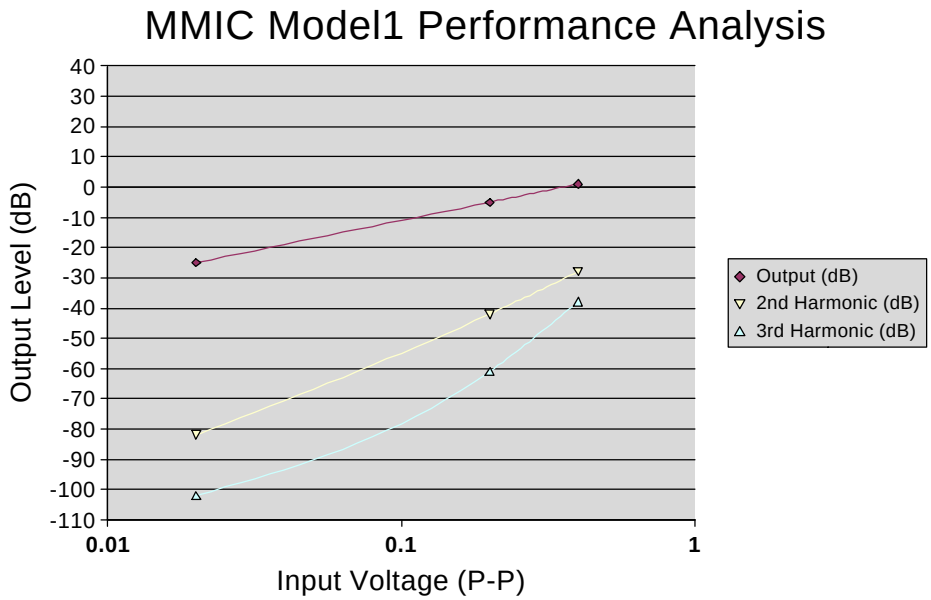

Figure 11

This EWB modeling confirms the previous observations that MMICs generate higher harmonics when driven with anything except very low levels.

4) Choices to be Made

What do these harmonic levels mean for an amateur radio VFO application? The builder has several options. The first would be to keep the drive levels very low and minimize the harmonics. However, these drive levels may be lower than what is required by most radio front ends.

Another option would be to replace the MMIC with a different type of amplifier having significantly better linearity. For example, a Norton lossless feedback amplifier or high performance op amp. Then the harmonics would again be be evaluated.

Still another option would be to drive the AD9854 at the higher level and use a low pass filter or band pass filter on the output to reduce the harmonics. Different filters would need to be selected for different frequency ranges.

In practice, filters will probably be required anyway.

Work to be Done

More experimentation is needed. These are some of the ideas that need testing:

1) Replace the MMIC with a different type of amplifier having significantly better linearity. For example, a Norton lossless feedback amplifier or high performance op amp.

2) Use band pass filters to further suppress spurious output. For multi-band operation, use relays to select different filters with appropriate frequency ranges.

3) Try the HFVFO in different applications – with active and passive mixers, etc.